On Fingerprint Processing Involving Modern Massively Parallel Architectures

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# Introduction

Fingerprint recognition is still the most widely accepted mean for a person identification and authentication. Two recent trends can be observed in automated fingerprint identification systems (AFIS): a shift towards mobile security systems and a querying the very large fingerprint databases (of order 106-107 and higher). Consequently two separate challenges arose in the field of fingerprinting: how to robustly identify a person with limited computational resources and how to speed up the database processing? The scalability problem is a long known issue in biometrics. With the number of records increasing so does the response time of the biometric system, and for a subset of AFIS, the real-time AFIS, the time is one of the quality characteristics.

In a generic AFIS there are following processing steps:

1. Image acquisition on a scanner
2. Image transmission from a scanner to the processing unit
3. Image enhancement (IE), can be omitted
4. Feature extraction and template building
5. Matching the template against database or part of it
6. Decision making whether to grant or deny the access given the matching results

In order to improve the overall system performance one should improve the performance of every step, which is usually obtained through the introduction of parallelism. A note should be taken that steps 1 and 2 usually don’t require speed up due to the hardware implementation of those steps, and their addition to a total processing time tends to be relatively small. As most systems implement step 6 in a form of a rule-based module with a single rule, the parallel implementation in this case might also be redundant.

With the hyperthreading and multi-core processors being available for some time now the simple way to improve the system performance was implemented in commercially available systems. The template database is chunked equally by the number of physical or logical cores and each chunk is processed independently, not unlike map-reduce approach or multi-agent systems. This approach is also scaled to the computing clusters, yet the price of such solutions is high. There exists a cheaper alternative. General Purpose Graphical Processing Unit (GPGPU) computations is now a proven way to enhance a system performance in HPC. Among the many GPGPU technologies (e.g. OpenCL, DirectCompute) NVIDIA CUDA is the most advanced and readily available.

In this paper we demonstrate our results of implementing various steps of AFIS processing using NVIDIA CUDA technology. The paper is organized as follows. In section 2 an overview of parallel fingerprinting algorithms research to date is given. A small overview of CUDA technology is provided in section 3. The discussion of various aspects in parallel fingerprint processing is given in sections 4 and 5 and a conclusion is made in section 6.

# Related works

Prabhakar and Kameswara in [1] propose a scheme of a coarse minutia-based matcher for filtering out stored fingerprint templates that are unlikely to match the query. The proposed scheme is a de-facto continuous classifier [2] with a percentage of matched minutiae serving as a point in a 1D space. Each feature of a query vector is loaded to a separate processor element (PE). Every feature of a stored vector is matched independently with every query feature. If at least one of the PE produces a positive result, total matched count is increased. However the algorithm is made in assumption that two fingerprints are already aligned in orientation and the core point is detected in both of them. Authors notice a convenience of Single Instruction Multiple Data (SIMD) architecture for implementing the algorithm.

A similar approach is proposed by Ratha and Jain in [3] and [4] for FPGA which are well known for their parallel capabilities. Additional steps are done to prevent the same feature from being matched more than once. Matching speed of 1.1·105 matches per second is reported. This algorithm uses the Hough transform for fingerprints alignment, although it is only stated that parallel implementation on the chosen FPGA is available. SIMD processor efficiency for the task is once again noted. Authors also make a statement about two levels of parallelism in matching algorithm: macro-level for inter-template matching and micro-level for intra-template matching.

Gowrishankar in [5] describes a scheme of a feature extraction algorithm for a binary skeletonized image based on the neighbor colored pixels count and proposes the usage of massively parallel architecture of a computing device due to the information being extracted from a small neighborhood around each pixel.

Bai et al. in [6] investigate the capabilities of a NVIDIA graphic boards supporting CUDA for the parallel implementation of a well-known FingerCode algorithm [7]. Authors use a slightly modified version of a FingerCode due to technological limitations of a chosen matching scheme, but report a performance of 2.03 million of matches per second. Our previous studies also indicate a great potential in FingerCode’s parallel implementation, especially after spatial characteristics optimization (band number, band width, innermost radius, fnumber of filters, number of sectors).

Cappelli, Ferrara and Maltoni report of a new local minutiae template based on a metric calculated for a minutiae around a sample one in a 3D lattice points inside a cylinder structure and its matching technique in [8] with a consequent consolidation step. The optimized version of such a template can be reduced to be a bit vector which can be efficiently matched with each other. Different approaches for consolidation step are then proposed. In a later press-release [9] authors state the increase of performance from 2.5 million mathes per second on a CPU to 4 million on a GPU.

# NVIDIA CUDA overview

The NVIDIA CUDA technology is used in a GeForce family of graphic boards [10]. Its programming model is shown on fig.1.



Fig.1. CUDA programming model

According to this model all computations are divided to CPU-based and GPU-based with CPU aliased as host and GPU as device. The host sends a program kernel – a compiled GPU shader – to the device. A thread configuration occurs on a device prior to the kernel execution. It is assumed a large number of threads will be created during execution and those threads are united as blocks. All threads of a single block are executed on a single device multiprocessor, and the threads in the block are physically united in the warps where instructions are executed simultaneously. The set of blocks makes a grid. Currently the number of threads in a warp is 32, the dimensionality of block and grid is not bigger than 3 with a limitation of a 1024 threads maximum per a single block. Up to 16 blocks with a total number of threads less than or equal to 2048 can be executed simultaneously on a single multiprocessor.

The CUDA technology allows the algorithms development for a powerful streaming processor with a possibility of a simultaneous computations in a several thousand threads at once. There are some notable limitations:

1. The block size should be chosen with a register memory consumption per thread in mind as its amount is limited in a multiprocessor.
2. Global memory I/O is recommended to be optimized in such a way that, simply put, threads with a neighboring indexes are accessing neighboring 4-bytes words. This will allow to access the data in batches instead of single word access for each thread.
3. It’s forbidden to use recursive functions.
4. Branching to different paths is executed slower than branching to a single path by all threads.

Therefore implementing some algorithms in CUDA might be difficult.

# Image enhancement and minutiae extraction

Image enhancement is a crucial step for real-time AFIS, as the impression quality is generally lower during system usage than during registration. Different methods were proposed to improve the quality of the acquired fingerprint, a survey can be found in [11]. It was shown that contextual enhancement is better than context-less enhancement, and Fronthaler, Kollreider and Bigun in [12] demonstrate the superiority of the pixel-wise enhancement versus block enhancement, e.g. it doesn’t produce artifacts at blocks’ borders.

The enhancement method involving Laplacian-like pyramid image decomposition and Linear Symmetry (LS) estimation proposed by Fronthaler, Kollreider and Bigun in [12] is also considered to be efficient if implemented on massively parallel architectures for the following reasons:

* It may be viewed as a sequence of transformations where each transformation uses only the previous results to obtain the next one – every transformation is non-iterative.
* Every transformation operates on a 2D matrices in such a way that each element’s computation is independent from the computation of other elements other than by the source data, which is immutable.
* Furthermore, most of the transformations include 2D convolutions, either ordinary or complex, that can be efficiently parallelized [10], and most kernels contain gaussians, so their separability property may as well be used.

In our studies we’ve implemented convolutions in a straightforward way without using separability due to the relatively small size of the kernels and the memory access pattern while a parallel processing was done on an element level. Thus our timings can further be improved. The size of Gaussian kernels is determined using a “3 sigma” rule by a formula . It could also be observed that amount of operations per pixel is constant, so the processing time is a linear function from the amount of pixels in the image or, in other words, image area. Parameters used a summarized in table I, and timings are shown in table II.

TABLE I

Parameters for image enhancement routine

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| σ1 | 0.6 | f0 | 1.7 | f2,f3 | 1.3 | τ2 | 0.3 | σdirections | 2.0 |
| σ2 | 3.2 | f1 | 1.21 | τ1 | 0.1 | Annulus radii | Inner 4, outer 6 | Number of directions | 20 |

TABLE II

Image enhancement time on different graphic boards

|  |  |  |
| --- | --- | --- |
| Database (resolution) | NVIDIA GeForce 560, ms | NVIDIA GeForce 570 |
| FVC2000 DB2 (256 x 364) | 20 | 15 |
| FVC2004 DB1 (640 x 480) | 60 | 43 |

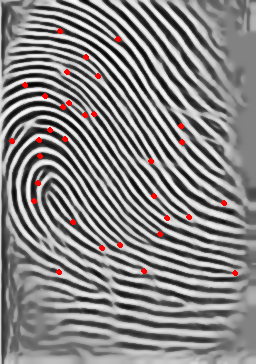
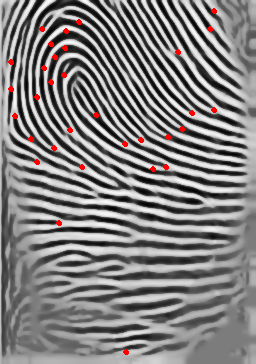
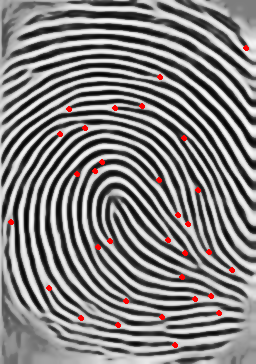


Fig.2. Enhanced versions of the FVC 2000 DB2 fingerprints with a minutia marked a) 1\_2 b) 80\_1 c) 80\_3

Minutiae extraction, also described in [12] is performed afterwards. LS and Parabolic Symmetry (PS) are estimated in order to produce the final measure PSi(x,y) = PS(x,y)\*(1-|LS(x,y)|). The area of each local maximum (Xm, Ym) is checked for a consistent high LS, and the list of maximums is then sorted by a descending |PS(Xm, Ym)| as a certainty measure resulting in a minutiae list. For the reasons described below we’re storing only top 32 minutiae as a template. Convolutions and local maximum estimations are implemented in parallel while the minutiae list generation and sorting is done sequentially. Generally, those operations are lightweight compared to LS and PS estimation. Table III contains the parameters of the process being used. Those parameters should be chosen carefully in order to minimize the amount of spurious minutiae. However we’ve observed a consistency in their detection among different impressions of the same finger (fig. 2). The timings are shown in Table IV.

TABLE III

Parameters for minutiae extraction routine

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| σ1 | 0.6 | f0 | 1.7 | f2,f3 | 1.3 | τ2 | 0.3 | σdirections | 2.0 |
| σ2 | 3.2 | f1 | 1.21 | τ1 | 0.1 | Annulus radii | Inner 4, outer 6 | Number of directions | 20 |

TABLE IV

Minutiae extraction time on different graphic boards

|  |  |  |
| --- | --- | --- |
| Database (resolution) | NVIDIA GeForce 560, ms | NVIDIA GeForce 570 |
| FVC2000 DB2 (256 x 364) | 25 | 20 |
| FVC2004 DB1 (640 x 480) | 75 | 50 |

# Minutia-based fingerprint matching

Minutiae-based fingerprint matching is a cornerstone of a modern AFIS. As noted in [3], database matching can be done in parallel on 2 levels: micro-level where different minutiae are matched in parallel with a given one and macro-level where different fingerprints are matched in parallel. However we need to point out that in [1], [3] and [4] are operating on an already aligned set of fingerprints, and that may not be the case for a real-time AFIS. Fingerprint alignment is a difficult task that can be formulated in a following way: given two fingerprint templates t1 and t2 what are the best parameters for translation and rotation to maximize the matching score? A detailed survey of the developed methods can be found in [11].

In our approach we’re assigning one CUDA block to each of the database fingerprints so it scales naturally on different and more advanced graphic boards. Each block consists of 32x32 threads, and currently it is the technological maximum for CUDA. Thus we’re limiting the template size to 32 minutiae. Both query template Q {qi} and database template D {di} are loaded to the cache memory of a multiprocessor. After that for every minutia qn and dk in these templates a template copy (Qn {qni} and Dk {dki} accordingly) is made and translation is done to make the minutia qnn and dkk coordinates equal to (0;0), so indices n and k can be used to indicate translation parameters. The thread Tij then uses a Qi and Dj templates to calculate the possible rotational alignment.

First, we’re assuming that fingerprints are already coarsely rotationally aligned by a scanner, that is, it’s acquisition window or similar sensor is designed in a way that makes it difficult or inconvenient to acquire a rotated fingerprint, which is usually the case for modern scanners. For every minutiae pair in (qim∈Qi\qii; dil∈ Dj\djj) the difference between Euclidean distances and is computed. After that the slope angles of and and their difference Thetaimjn are calculated. If distance difference and angle difference are below certain thresholds, (I, j, Thetaimjn) is considered to be a plausible alignment parameters and is stored in a cache memory.

The second step is matching two fingerprints given a set of plausible alignment parameters. The set is distributed equally among 1024 working threads. Matching procedure is similar to the one described by Wegstein in [], but it uses Euclidean distance differences instead of coordinate differences. Due to the constant amount of the minutiae in the templates the thread output is a number of the matched minutiae. Its maximum is searched among all thread outputs (and consequently among all the alignment parameters) and is considered to be the final matching score.

FVC 2000 DB2 was used in conjunction with image enhancement and minutiae extraction technique discussed earlier to obtain the quality results for a proposed approach for 3960 genuine and 386760 impostor matches. Its quality characteristics are displayed in Fig. 3. We report an average time of 0.41 ms for a single fingerprint match.

Fig.3 FAR and FRR

# Discussion and conclusion

Our results demonstrate that filter-based and. Despite our focus on a direct grayscale minutiae extraction, GPGPU usage is also a perspective approach for a skeleton-based techniques, as there are GPU-accelerated ways for producing image skeletons [Вот эти ребята], and minutia extraction from them (e.g. [5]) is highly parallelizable.

As for the minutiae matching, the matching speed is much lower than one could expect from a massively parallel architecture implementation. First of all, there’s definitely a place for a further optimizations in the implemented algorithm. Secondly, the alignment step of our approach is a “brute force” search which can produce several thousand of possible alignments. Despite the fact this algorithm and matching procedure are highly parallelizable by data, internally they’re implemented in a sequential manner due to the lack of a single block resources. Thus with a finer alignment algorithm resulting in a lesser amount of possible alignment parameters a noticeable speedup is expected. It should also be noted that with a pre-alignment step the implementation of a micro-level parallelism for minutiae matching on CUDA is a straightforward decision.

Another concern is the recognition quality the amount of minutiae being used. 32 minutiae is, on average, only 50 to 75% of its total amount in a given fingerprint. Yet from the ROC one is able to devise a FAR=0.001% at a price of FRR=25%. While some fingerprints in a database contain unrecoverable regions, we consider the spurious minutiae to be the core reason of the high FRR, as any amount of false minutiae in a limited size template worsens the recognition quality. It is another field for improvement.

The code for the algorithms discussed is available at <http://code.google.com/p/cuda-fingerprinting/> and requires CUDA 2.0 compatible graphic board to run.

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